

CLAIMS

What is claimed is:

- 1 1. A method to efficiently design and implement a matched
2 instruction set processor system, including:
 - 3 decomposing the matched instruction set processor system into
4 interconnected design vectors, each of the interconnected design vectors
5 including a binding header method, a run method, a conjugate virtual machine
6 (CVM), a binding trailer method, and an invocation method; and
7 analyzing and mapping the interconnected design vectors into a re-
8 configurable platform.
- 1 2. The method of claim 1, wherein analyzing and mapping the
2 interconnected design vectors includes:
 - 3 mapping the interconnected design vectors into a pre-synthesis re-
4 configurable platform.
- 1 3. The method of claim 2, wherein analyzing and mapping the
2 interconnected design vectors includes:
 - 3 transforming the pre-synthesis re-configurable platform into actual
4 hardware through a physical realization process.
- 1 4. The method of claim 1, wherein analyzing and mapping the
2 interconnected design vectors includes:
 - 3 mapping the interconnected design vectors into a post-synthesis re-
4 configurable platform.
- 1 5. The method of claim 4, wherein mapping the interconnected design
2 vectors includes:

3 configuring the post-synthesis re-configurable platform at compile-time to
4 match processing requirements of specific applications.

1 6. The method of claim 5, wherein configuring the post-synthesis re-
2 configurable platform at compile-time includes:

3 using the CVM of each interconnected design vector to specify required
4 attributes and capabilities; and

5 configuring the post-synthesis re-configurable platform at compile-time to
6 match the required attributes.

1 7. The method of claim 6, wherein configuring the post-synthesis re-
2 configurable platform at compile-time includes:

3 using the CVM of each interconnected design vector to specify required
4 attributes; and

5 configuring the post-synthesis re-configurable platform at compile-time to
6 match the required attributes.

1 8. The method of claim 7, wherein configuring the post-synthesis re-
2 configurable platform at compile-time includes:

3 using the CVM of each interconnected design vector to specify required
4 attributes, the required attributes including logic, placement, and routing
5 information; and

6 configuring the post-synthesis re-configurable platform at compile-time to
7 match the required attributes.

1 9. The method of claim 4, wherein mapping the interconnected design
2 vectors includes:

3 configuring the post-synthesis re-configurable platform at run-time to
4 match processing requirements of specific applications.

1 10. The method of claim 9, wherein configuring the post-synthesis re-
2 configurable platform at run-time includes:

3 using the CVM of each interconnected design vector to specify required
4 attributes; and

5 configuring the post-synthesis re-configurable platform at run-time to
6 match the required attributes.

1 11. The method of claim 10, wherein configuring the post-synthesis re-
2 configurable platform at compile-time includes:

3 using the CVM of each interconnected design vector to specify required
4 attributes, the required attributes including a set of re-programmable parameters
5 having values that can be downloaded and changed at run-time; and

6 configuring the post-synthesis re-configurable platform at compile-time to
7 match the required attributes.

1 12. A system to efficiently design and implement a matched instruction
2 set processor system, including:

3 an architectural modeling unit to decompose the matched instruction set
4 processor system into interconnected design vectors, each of the interconnected
5 design vectors including a binding header method, a run method, a conjugate
6 virtual machine (CVM), a binding trailer method, and an invocation method; and

7 a realization mapping unit operatively coupled to the architectural unit to
8 analyze and map the interconnected design vectors into a re-configurable
9 platform.

1 13. The system of claim 12, wherein the realization mapping unit maps
2 the interconnected design vectors into a pre-synthesis re-configurable platform.

- 1 14. The system of claim 13, wherein the realization mapping unit
2 transforms the pre-synthesis re-configurable platform into actual hardware
3 through a physical realization process.
- 1 15. The system of claim 12, wherein the realization mapping unit maps
2 the interconnected design vectors into a post-synthesis re-configurable platform.
- 1 16. The system of claim 15, wherein the realization mapping unit
2 configures the post-synthesis re-configurable platform at compile-time to match
3 processing requirements of specific applications.
- 1 17. The system of claim 16, wherein the realization mapping unit uses
2 the CVM of each interconnected design vector to specify required attributes and
3 capabilities, and the realization mapping unit configures the post-synthesis re-
4 configurable platform at compile-time to match the required attributes.
- 1 18. The system of claim 16, wherein the realization mapping unit uses
2 the CVM of each interconnected design vector to specify required attributes, and
3 the realization mapping unit configures of the post-synthesis re-configurable
4 platform at compile-time to match the required attributes.
- 1 19. The system of claim 17, wherein the realization mapping unit uses
2 the CVM of each interconnected design vector to specify required attributes, the
3 required attributes including logic, placement, and routing information, the
4 realization mapping unit configures of the post-synthesis re-configurable
5 platform at compile-time to match the required attributes.

1 20. The system of claim 15, wherein the realization mapping unit
2 configures the post-synthesis re-configurable platform at run-time to match
3 processing requirements of specific applications.

1 21. The system of claim 20, wherein the realization mapping unit uses
2 the CVM of each interconnected design vector to specify required attributes, and
3 configures the post-synthesis re-configurable platform at run-time to match the
4 required attributes.

1 22. The system of claim 21, wherein the realization mapping unit uses
2 the CVM of each interconnected design vector to specify required attributes, the
3 required attributes including a set of re-programmable parameters having values
4 that can be downloaded and changed at run-time, and the realization mapping
5 unit configures the post-synthesis re-configurable platform at compile-time to
6 match the required attributes.

1 23. A machine-readable medium comprising instructions which, when
2 executed by a machine, cause the machine to perform operations comprising:
3 decomposing the matched instruction set processor system into
4 interconnected design vectors, each of the interconnected design vectors
5 including a binding header method, a run method, a conjugate virtual machine
6 (CVM), a binding trailer method, and an invocation method; and
7 analyzing and mapping the interconnected design vectors into a re-
8 configurable platform.